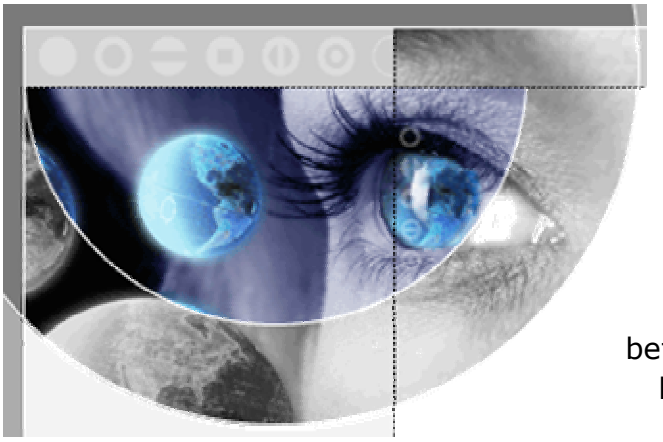


NanoScope Services – Application Note

A guide to preparing a Circuit Edit job

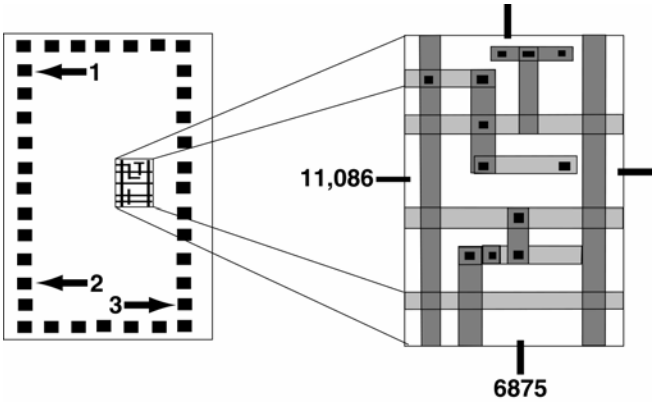
When have devices modified, either during a visit or remotely by courier, preparing the correct information beforehand saves time, allows for effective discussion on best practice, and minimises the FIB intervention cost.

A FIB system uses a highly accurate sample stage, which can be mapped onto the device co-ordinate system. This permits direct navigation to each intervention site. Once there, the local metal structures are used to precisely position further operations.
But - devices appear almost totally different when seen in a design tool or when seen under a FIB. For example - the FIB image can normally only image the top metal layer and the probe pads. IN addition many fully planarised devices offer no visible layout features at all, so local lock-points need to be exposed by FIB milling near each intervention site – detailed navigation information is therefore essential.

This may be provided in several ways.
1) Supplying locking and modification co-ordinates and some annotated plots
2) Supplying an edited GDSII file with modification annotations.

For 1) Co-ordinates and Plots

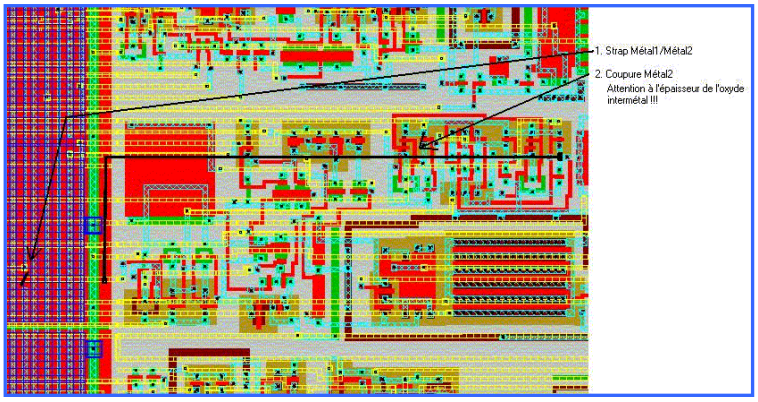
The first data required are at least 3 orthogonally opposite locking points.
These points set the scaling of the device in X and Y, correct any scaling differences on the physical device, correct for any rotation or skew effects, and allow direct navigation to any location on the device without imaging.
Each point selected must be visible on each devices requiring work, and not obscured by bond wires or parts of the packaging (partially de-capsulation). A good choice is normally the inside corners of bond pad openings. Here shown numbered TPA1 to TPA3.



Three-Point-Alignment	X	Y	
TPA-1	300	15900	
TPA-2	900	1400	Bond Pad Corner
TPA-3	9700	1200	Bond Pad Corner
Cuts and Straps			
C-1	6879	11090	M2
C-2	6875	11084	M1
S-1a	6884	11090	M1
S-1b	6884	11082	M1
S-2a	6878	11085	M1
S-2b	6884	11085	M2

It is important to identify exactly which corner has which co-ordinate (top right is not the same as right top for example). It is sometimes helpful to provide images and annotate them clearly.

The next step is to provide annotated plots of the area of each intervention and to add a sketch of the intervention to the plot – this also helps the layout engineer visualize how the fix will appear on the final device.



It is helpful to the FIB engineer if these plots are prepared in a certain way –

1) Remove all layers which are not metal layers (like interconnects, n or p-wells, oxide windows, or polysilicon)
2) Remove all metal layers that are lower than the lowest target structure required by the fix (so if the deepest via connection is to metal 3 then remove metals 2 and 1 also) This de-clutters the layout plots and allows the operator to quickly interpret the structures as they become visible in the FIB instrument.
3) Add a legend – a chart identifying which colour each metal layer has (It is helpful to also know the expected thickness of each metal layer.
4) Several plots of the target area at different magnifications – this allows the operator to locate nearby top layer metal and use this to navigate directly to the intervention site.
5) Each image should have a scale bar and the structures nearest the intervention should have some measurements added (width of, or distance to, nearby tracks for example) – so that relative measurements can be taken and used for navigation at the site.
6) A white rather than a black background is also helpful as the plots often need to be printed and annotated during the fix.

If the plots can be sent ahead of the work this would allow us to review the intended fix and point out potential problems and suggest alternatives to keep the yield at a maximum and the cost (time) of intervention to a minimum. The process of reviewing and understanding your exact requirements also enables us to produce an exact quotation based on that understanding.

For 2) Annotated GDSII files

When supplying a GDSII file instead of co-ordinates and plots, it is necessary to add annotations and to supply some additional information -

1) The exact layer names of metal and poly-silicon layers (these MUST be case and space specific)
2) Exact layers numbers of metal and poly-silicon process layers.
3) The TOPCELL name (case and space specific)
4) The interventions required should be added as an additional metal layer in the GDSII and the same information supplied for that layer as above. A short description of what each intervention is to achieve is also highly useful.
5) It is helpful if the GDSII file is kept to an easy-to-handle size to save handling time.
6) It is not necessary to include all the device layers as with 1), but these can also be switched off in the GDSII viewer if removing them is too time consuming and the file size is not too large.

Tips to maximize yield and minimize cost

Many complex interventions are possible, and NanoScope specialises in the most challenging work on the most advanced processes – but there are always several ways to achieve a specific result, and it is always advisable to start with best practice.
These simple guidelines are you help you design your fix for speed and yield. We are happy to consult and advise you during this process and to offer alternative suggestions.

When selecting a via point

- The lower the metal layer, the longer and more difficult it is to connect to. This is not just because of the time taken to mill through the higher layers, but because of the care needed to avoid all other structures on the way down. As a guide on a typical 7 metal process - M7=2 mins, M6=8 mins, M5=14 mins, M4=20 mins etc.
- Pick a location where the target track is not covered by higher metal layers – this is not always possible. If not then try to pick a site near the edge of a higher metal track, and where it is only covered by 1 higher metal layer.

When adding new tracks

- The longer the track the longer the deposition time, as a guide – 10um=10 mins, 50um's=15mins, 100um's=20mins, 500um's=45mins.
- If new tracks (especially long ones) are needed in close proximity, clean up time can become important – try to keep tracks as far apart as possible.
- If track resistance is important (NanoScope recommend W for the lowest ohm/min option) it may be necessary to increase the volume of a track – please consult with us for this.

When cutting tracks

- The lower the metal layer the longer the time required to cut it and the higher the risk of secondary effects – try to keep cuts in the higher metal layers.
- Pick a cut location where the target track is not covered by higher metal layers. If this is not possible, try to pick a location near the edge of a higher metal track, and where it is only covered by 1 higher metal layer.
- Try to position cuts a minimum distance of 5 microns away from new connections.

General points to consider.

Each operation has a yield (sometimes its 99.99%) but yield is cumulative – therefore 20 operations at 99% is 82%. Try to separate the fixes onto different devices to prove the functionality to maximize yield.
Devices should ideally not be modified if they have not tested as 'functional', as this means poor yield may be due to a wide number of reasons.
We normally recommend doing 3 of any fix for an accurate understanding of the result – if any two devices behave the same, then the fix was 'good' even if sometimes the result was not the expected one.
Many faults with devices are not completely understood at the time of intervention, one way to check if the intervention was correct or not, is to reverse it and see if the original behaviour is re-established.