NanoScope Services
FIB Technology Made Easy

FIB assisted electrical debug (micro-probing your layout) for 1st Silicon (part of the NanoScope 'Summer of Love' rel1.1- 28 June 2018)

An often overlooked option in the race to get 1st Silicon devices working, is simple electrical probing (µm), but why is this?

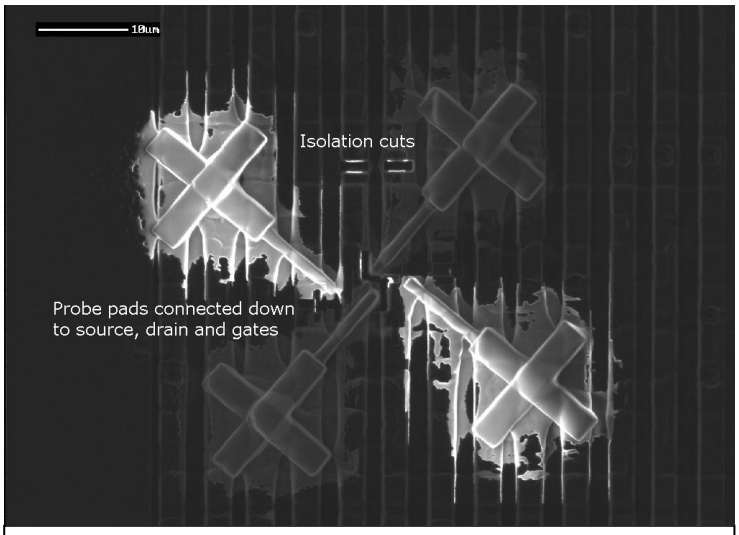


Image - Floating and grounded probe pads connected to gates, source and drain of a transistor pair.

Well the reasons are all very human. We think because line-widths are getting smaller and top down access to (often) buried nodes is almost impossible (for anything that's not top layer metal), that this technique is simply not applicable now.

So the questions and options we consider run along these lines

"How can I get through a WL-CSP package (for example) and get a needle onto a buried node to find the state of that node? Impossible, right?

And the track is only 90nm's wide anyway, so the probing station I will need will not only be extremely expensive to buy/rent/use, but could be far away, meaning I'll have to travel and possibly spend a couple of days trying to get that to work.

And even if everything goes well, it's likely it won't give me a clean contact and a clear answer which will be difficult to explain, even if I can get a needle down without breaking the circuit right away.

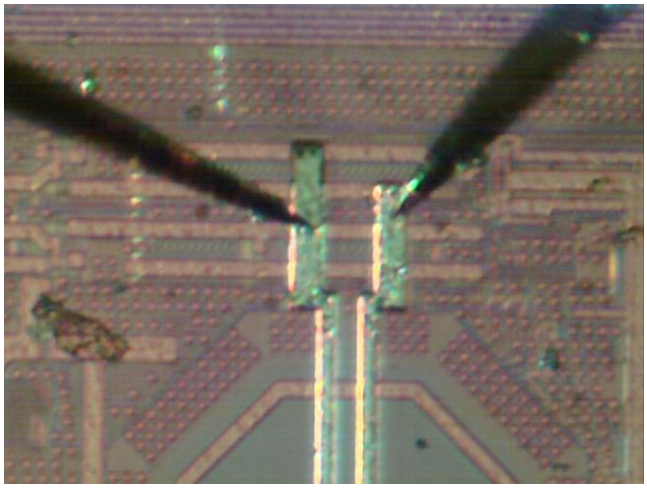
And I'll have to explain and justify this whole risky process to the project leader who's not going to like it when I come back with half an answer, a big invoice to go with it and 2 weeks lost as well."

So instead of all that pain, it's quite human of us to just say – "let's just model it to death and then gamble on a mask change" – isn't that the way it has to go now?

Well no actually – it's quite possible to directly probe almost any node, buried or not, and with quite simple, even crude, probing equipment.

AND it's not really important that the nodes and linewidths are smaller than even very small probes – because it's not necessary to touch them directly in the first place.

We just need to add a little FIB to the mix. (Focused Ion Beam) FIB is a normal technique for testing layout changes before committing to a mask change and 2nd Silicon - and an expert FIB service labs like ours, specialise in turning around small lots for testing and demos in very short time frames.



In fact the harder the fix the more interesting it is for us – if every postdoc at a University Physics dept using an analytical FIB could get our nano-surgery success rates, it would soon become boring.

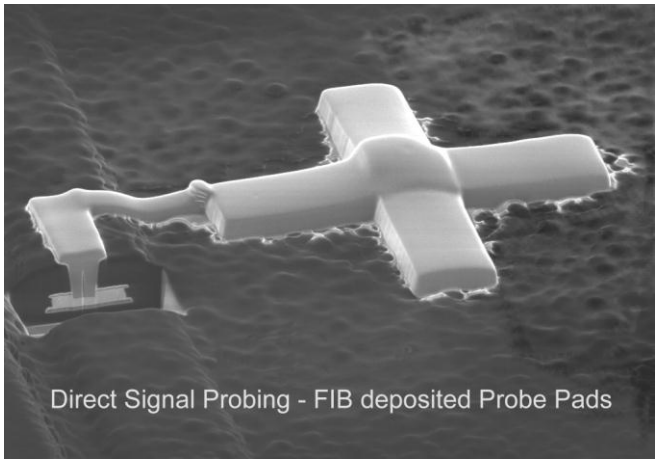
We've been doing this (wearing one hat or another) since 1992 and I'm proud our client base comes from as wide a variety of chip designers as it's possible to think of – from CERN LHC detector electronics for looking at the very smallest part of our Universe, to space instrument control systems for looking at the largest.

It's all been in our FIBs – and that's just the Circuit Edit/Nano-surgery jobs, not Failure Analysis or Nano-Engineering or TEM sectioning for materials analysis.

So – not only can various net-list modification theories be directly checked – by using a FIB to disconnect/reconnect nodes deep inside a 1st Silicon design, but there is an additional way to accelerate this process.

It's very simple; you CAN probe your 'difficult to get at' node directly – and find out which theory is true and design your layout fix directly based on that.

Just use our FIB to contact down to your buried node, and then put down a nice juicy probe pad, right where you can get at it with a very standard needle.



The likelihood of getting a probe down with this in place in even a normal lab environment is high, the equipment needed is low cost, plentiful, and easy to find (ish), and you can learn a lot about your circuit in a just a few minutes.

Now you can decide what to do – you can find out how the circuit is behaving at that node by measuring it directly, or alternatively you can intervene in the circuit behaviour. By forcing an input to a known state (for example) you can directly confirm that the rest of the downstream circuit is behaving normally (or not), giving you the confidence to implement a fix or refine it.

If we decap the chip on the board (often possible) then you can just bring your laptop and a few cables and run your standard tests at the same time.

We've recently refurbished a legacy probing station (with optical microscope) to do just this, and its sitting right next to our FIB for IC nano-surgery and a curve tracer – so don't be shy.

Our customers making layout changes often bring test equipment with them to check fixes as we make them, so adding a little light probing for inaccessible nodes is just the next logical step.

So when 1st Silicon isn't quite behaving itself, and the reasons are not quite modelling out in a convincing way, there is a sometimes overlooked but effective way to put your finger (probe) on the reason – and it's a lot easier to explain and justify than you might think. (learn more here)

Lets start a conversation this summer – we're ready to talk

With kind regards, Lloyd

Lloyd Peto

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